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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/687,858	10/13/2000	Chak Cheung Edward Ho	0100.0000780	8827

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EXAMINER
CHANG, ERIC

ART UNIT	PAPER NUMBER
2185	3

DATE MAILED: 08/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/687,858	EDWARD HO ET AL.	
	Examiner	Art Unit	
	Eric Chang	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-18 are pending.

Drawings

2. The drawings are objected to because figure labels "Strobe 1 for Signal Pad 1" and "Strobe 1 for Signal Pad K" in FIGS. 1 and 3 overlap other figure elements. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because of undue length. Correction is required. See MPEP § 608.01(b).

Claim Objections

5. Claims 4-5, 8, 10-11, 13, 15-16 and 18 are objected to because of the following informalities: all instances of the term "mulitplexer" should instead read, "multiplexer" or "multiplexor". Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of U.S. Patent 6,067,272 to Foss et al.

8. As to claim 1, in the Background of the Invention section of the Disclosure, Applicant discloses as prior art a signal phase shifting circuit to shift the phase of an input signal, comprising:

[a] a reference signal period dividing circuit comprising a phase shift generator that receives a reference and a feedback control signal and outputs a delay control signal for a variable delay circuit [FIG. 1, element 22, and page 4, lines 1-14]; and

[b] a variable delay circuit to provide a phase shifted output of an input signal based on the delay control signal from the reference signal period dividing circuit [FIG. 1, element 28, and col. 4, lines 16-22].

Applicant teaches all of the limitations in the claim exist in the admitted prior art, but does not teach that a feedback delay matching circuit is coupled to the output of the phase shift generating circuit to produce the feedback control signal.

Foss teaches that a feedback delay matching circuit representing a delay model [col. 3, lines 63-67, and col. 4, lines 1-6] may be used in the construction of a delay locked loop [col. 2, lines 48-55].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ feedback delay matching means as taught by Foss. One of ordinary skill in the art would have been motivated to do so to reduce clock skew within a memory access system.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of clocking a memory system. Moreover, the feedback delay matching means taught by Foss would improve the flexibility of admitted prior art because it allowed the memory to operate at high speeds and maintain its capability as operating conditions vary.

9. As to claims 2, 4, 10 and 15, Applicant discloses as prior art the variable delay circuit includes a delay stage and at least one phase shifted output signal drive buffer [FIG. 1, element 40, and page 4, lines 16-22]. Applicant also discloses as prior art the variable delay circuit includes a multiplexer coupled to the delay stage [FIG. 1, element 42].

10. As to claims 3, 5, 11 and 16, Foss discloses the feedback delay matching circuit uses similar elements as the clock delay path [col. 3, lines 63-67, and col. 4, line 1]. Foss teaches that the clock delay path includes a plurality of serially coupled buffer stages, or a plurality of multiplexer and buffer stages [FIG. 5, elements 25 and 27, and col. 3, lines 36-45], to compensate for delay variations [col. 4, lines 1-6].

11. As to claim 6, Applicant discloses as prior art discloses a data latch having a first input to receive data and a second input coupled to receive the phase shifted output signal [FIG. 1, element 16, and page 3, lines 24-31].

12. As to claims 7, 12 and 17, Applicant discloses as prior art discloses the reference signal is a CLOCK signal, and the input signal is a STROBE signal [FIG. 1, elements 12 and 20, and page 3, lines 24-31], substantially as claimed.

13. As to claims 8, 13 and 18, Applicant discloses as prior art discloses the phase shift generating circuit includes a plurality of serially coupled buffers forming a controlled delay stage [FIG. 1, element 37]. Furthermore, Foss discloses the feedback delay matching circuit includes a plurality of serially couple multiplexer and buffer stages coupled to the controlled delay stage [FIG. 5, elements 25 and 27, and col. 3, lines 36-45].

14. As to claim 9, Applicant discloses as prior art discloses a signal phase shifting circuit substantially as claimed. Furthermore, Applicant teaches that the phase shift generating circuit

includes a DLL comprising a phase detection circuit, a charge pump, and a loop filter [FIG. 1, elements 30, 32, and 34, and page 4, lines 1-8].

15. As to claim 14, Applicant discloses as prior art discloses a signal phase shifting circuit substantially as claimed. Furthermore, Applicant teaches that the signal phase shifting circuit is used in a data receiving circuit [page 3, lines 24-31] that further comprises a data latch coupled to receive data and the phase shifted output from the signal phase shifting circuit [FIG. 1, element 16].

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ec
August 10, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100